IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application. Where claims have been amended and/or canceled, such amendments and/or cancellations are done without prejudice and/or waiver and/or disclaimer, and Assignee reserves the right to claim this subject matter in a continuing application:

1. (Currently Amended) An integrated circuit package comprising:

(a) an integrated circuit die having at least one integrated circuit etched thereon, the integrated circuit comprising elements which require theoretically negative reactive component values; and

(b) a housing containing said integrated circuit die, wherein said integrated circuit die is electrically coupled to said housing using at least one wire bond; and wherein [[each]] the at least one wire bond has an inductance associated therewith, and comprises a series inductor of a series inverter portion of an impedance inverter circuit; and wherein the negative reactive component values theoretically required by the integrated circuit are actually incorporated into the integrated circuit through the use of ~~wire bonds having pre-determined inductance values, wherein a series inductance value of the integrated circuit is realized by a pre-determined inductance value of a wire bond~~ the impedance inverter circuit.

2. (Currently Amended) The integrated circuit of claim 1, wherein the impedance inverter circuit ~~comprises an impedance inverter having a~~ series ~~inductance value~~ inverter portion comprises a series inductance value, wherein the series inductance value of the impedance inverter circuit is realized by the pre-determined inductance value of a wire bond.

3. – 41. (Cancelled)

42. (New) The integrated circuit of claim 1, further comprising a first inductor electrically coupled to the series inverter portion at a first node, wherein the first inductor is arranged in a shunt arrangement.

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43. (New) The integrated circuit of claim 42, further comprising a second inductor electrically coupled to the series inverter portion at a second node, wherein the second inductor is arranged in a shunt arrangement.

44. (New) The integrated circuit of claim 43, wherein at least one of said first and second inductors are formed external to said integrated circuit.

45. (New) The integrated circuit of claim 43, wherein one of said first and second inductors is formed external to said integrated circuit and the other of said first and second inductors is formed integrally with said integrated circuit.

46. (New) The integrated circuit of claim 43, wherein each of said first and second inductors is formed integrally with said integrated circuit.

47. (New) The integrated circuit of claim 43, wherein each of said first and second inductors form a spiral inductor.

48. (New) The integrated circuit of claim 43, wherein said series inductor, said first and said second inductors form an impedance inverter adapted to transform a lower output impedance into a higher output impedance.

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